Yegun (Eric) Shim

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Education

University of Illinois at Urbana-Champaign — ***Expected Graduation:*** *May 2027*
Bachelor of Science in Computer Engineering — **GPA:** 3.91/4.0

- Dean's List (Spring 2025)
- James Scholar (Spring 2025, Fall 2025, Spring 2026)

Research Experience

Undergraduate Research Assistant, UIUC — **Champaign, IL**
Dafny-HLS Verification Research — May 2025 – December 2025

- Designed Dafny verification methodologies to reliably detect HLS-relevant bug classes in numerical kernels.
- Produced and annotated **~1,300 bug-injected Dafny benchmarks**, then benchmarked numeric behavior via Python analysis to support controlled LLM-based repair evaluation.

OpenRTLSet V2 Research — December 2025 – Present

- Contributed to **OpenRTLSet V2 (~500k RTL modules)**, a hierarchy-aware dataset for LLM-based hardware design.
- Performed module-type classification and verification for VerilogTypeEval benchmarking.
- Supported dependency-aware LLM labeling, evaluating hierarchy-serialization choices.

Ministry of National Defense, Republic of Korea — **Gangwon, South Korea**
Frontline Surveillance and Maintenance — November 2022 – April 2024

- Maintained 24/7 camera-based surveillance and secure networking systems; applied schematics-driven diagnostics and collected field data for AI surveillance model development.

Project

School Run — 2.5D FPGA Runner Game Engine — **Champaign, IL**
FPGA & SoC Designer — November 2025 – December 2025

- Designed a **MicroBlaze SoC** with DDR3 double-buffered framebuffer and custom **HDMI & renderer IP**.
- Implemented **AXI4-Lite & AXI4-Full** and a line-buffered sprite pipeline, integrating C game logic + RTL for real-time rendering.

FPGA CNN Accelerator — **Champaign, IL**
FPGA Accelerator Engineer — December 2025 – January 2026

- Built an **end-to-end MNIST inference pipeline** integrating RTL CNN accelerator, MicroBlaze firmware, and **web UI** (UART-based I/O).
- Achieved a **3339x speedup**, reducing end-to-end latency from **~454 ms to 0.136 ms**.

Neural Segmentation (3D U-Net) — **Champaign, IL**
ML Pipeline Engineer — August 2025 – Present

- Built the data preprocessing pipeline for multi-channel AAV microscopy using open-source tooling.
- Supported **3D U-Net training** and **fine-tuning** on NCSA GPU resources and integrated segmentation post-processing.

Involvement

KSEA (Korean Scientists & Engineers Association) Illinois — **Champaign, IL**
Active Member — May 2025 – Present

- CS subteam for neuron segmentation research in collaboration with faculty mentors.
- Collaborate in a cross-functional team (CS and BioE) on dataset preparation and model training experiments toward milestone-driven deliverables.

Skills & Interests

Skills: Verilog/SystemVerilog, AXI4 (Lite/Full), BRAM/DDR3, MicroBlaze, C/C++, Python, Vivado, Verilator, Linux, Git

Interests: Hardware Acceleration, Embedded Systems, SoC Architecture, FPGA & ASIC Design, HW-Aware Machine Learning